WHAT IS CLAIMED IS:

1. A synchronizing pattern position detection circuit comprising:

a plurality of selector circuits connected in a hierarchical arrangement,

each of the selector receiving two of synchronizing pattern detection signals and two of synchronizing pattern position signals and selecting one of the two of synchronizing pattern detection signals and one of the two of synchronizing pattern position signals,

one of the selector circuits located at an uppermost stage of the hierarchical arrangement outputting a finally selected one of the synchronizing pattern detection signals and a finally selected one of the synchronizing pattern position signals,

the synchronizing pattern signals being included in serial data,

the synchronizing pattern position signals indicating positions of the synchronizing pattern signals on parallel data obtained by a serial-to-parallel conversion of the serial data.

2. The synchronizing pattern position detection circuit as claimed in claim 1, wherein the plurality of selector circuits in the hierarchical arrangement are $[2^{m-1} + 2^{m-2} + \ldots +1]$ (m is an integer equal to or greater than 2) selector circuits in a case where the serial data is transmitted in a frame

unit having a data length of 2^m x n bits and converted into parallel data of a 2^m-bit width.

3. The synchronizing pattern position detection circuit as claimed in claim 1, wherein the hierarchical arrangement has given priority assigned to the plurality of selector circuits.

4. The synchronizing pattern position detection signal as claimed in claim 1, wherein each of the selector circuits selects one of the two of synchronizing pattern position signals based on values of the two of synchronizing pattern detection signals.

5. The synchronizing pattern position detection signal as claimed in claim 1, wherein:

each of the selector circuits includes an OR circuit that performs an OR operation on the two of synchronizing pattern detection signals; and

an output of the OR circuit corresponds to said one of the two of synchronizing pattern detection signals.

6. The synchronizing pattern position

detection circuit as claimed in claim 1, wherein:

each of the selector circuits has a first input terminal group that receives one of the two of the synchronizing pattern position signals, and a second input terminal group that receives the other one of the two of the synchronizing pattern position signals;

each of the selector circuits selects either the first input terminal group or the second input terminal group in accordance with the two of the synchronizing pattern detection signals.

7. A synchronizing pattern position detection circuit receiving synchronizing pattern detection signals and synchronizing pattern position signals indicating positions of the synchronizing pattern detection signals in parallel and detecting a position of a synchronizing pattern on parallel data, said synchronizing pattern position detection circuit comprising:

selector circuits connected in a hierarchical arrangement,

each of the selector circuits comprising first and second input parts for receiving synchronizing pattern detection signals, and third and fourth input parts for receiving synchronizing pattern position signals,

each of the selector circuits selectively outputting:

a synchronizing pattern position signal applied to the third input part when only a synchronizing pattern detection signal applied to the first input part indicates a given detection value or the synchronizing pattern detection signals

applied to the first and second input parts indicate the given detection value;

a synchronizing pattern position signal applied to the fourth input part when only a synchronizing pattern detection signal applied to the second input part indicates the given detection value; and

a synchronizing signal detection signal obtained by performing an OR operation on the synchronizing pattern detection signals applied to the first and second input parts.